Microprocessor

1) After CPI instruction is executed,if carry flag is set and zero flag is reset,then
a) data is equal to Accumulator content
b) data is greater than Accumulator content
c) data is less than Accumulator content
d) None of the above
= Answer (b) data is greater than Accumulator content

2) The instruction XCHG exchanges the contents of …….. register pair with the contents of …….. register pair.
a) PC and HL b) BC and DE c) DE and HL d) BC and HL
= Answer (c) DE and HL

3) NOP instruction is used to
a) replace the existing instruction
b) insert the delay
c) debug the program
d) All of the above
= Answer (d) All of the above

4) The contents of the Accumulator in an 8085 microprocessor is altered after the execution of the instruction.
a) CMPC b) CPI 3 A c) ANI 5C d) ORA A
= Answer (c) ANI 5C

5) In an 885 microprocessor,after the execution of XRA A instruction
a) the carry flag is set
b) the Accumulator contains FF_H
c) the zero flag is set
d) the Accumulator contents are shifted left by one bit
= Answer (c) the zero flag is set

6) In a microprocessor,the address of the next instruction to be executed,is stored in
a) stack pointer b) address latch
c) program counter d) general purpose register
= Answer (c) program counter

7) The computer program which converts statements written in high level language to object code is known as
a) assembler b) operating system
c) object-oriented software d) None of the above
= Answer (d) None of the above

8) Which one of the following is not a vectored interrupt?
a) TRAP b) INTR c) RST 7.5 d) RST3
= Answer(d) RST3

9) When a program is being executed in an 8085 microprocessor,its program counter contains
a) the number of instructions in the current program that have already been executed
b) the total number of instructions in the program being executed
c) the memory address of the instruction that is being currently executed
d) the memory address of the instruction that is to be executed next
= Answer (d) the memory address of the instruction that is to be executed next

10) The 8085 assembly language instruction that stores the contents of H and L registers into the memory locations 2050H and 2051H,respectively,is
a) SPHL 2050H b) SPHL 2051H c) SHLD 2050H d) STAX 2050H
= Answer (c) SHLD 2050H

11) In an 8085 microprocessorthe instruction CMP B has been executed while the content of the accumulator is less than that of register B.As a result
a) carry flag will be set but zero flag will be reset
b) carry flag will be reset but zero flag will be set
c) both carry flag and zero flag will be reset
d) both carry flag and zero flag will be set
= Answer (a) carry flag will be set but zero flag will be reset

12) In an 8085 microprocessor,the instruction CMP B has been executed while the ontents of accumulator is less than that of register B.As a result carry flag and zero flag will be respectively
a) set,reset b) reset,set c) reset.reset d) set,set
= Answer (a) set,reset

13) In an 8085 microprocessor system with memory mapped input,
a) input devices have 16 bit addresses
b) input devices are accessed using in and out instructions
c) there can be a maximum of 256 input devices and 256 output devices
d) arithmetic and logic operations can be directly performed with the input data
= Answer (b),(c)

14) In a microprocessor,WAIT states are used to
a) make the processor WAIT during a DMA operation
b) make the processor WAIT during an interrupt processing
c) make the processor WAIT during a power shunt down
d) interface slow peripherals to the processor
= Answer (a) make the processor WAIT during a DMA operation

15) When a CPU is interrupted,it
a) stops execution of instructions
b) acknowledge interrupt and branches subroutines
c) acknowledge interrupt and continues
d) acknowledge interrupt and waits for the next instruction from the interrupting device
= Answer (b) acknowledge interrupt and branches subroutines

16) A DMA transfer implies
a) direct transfer of data between memory and Accumulator

b) direct transfer of data between memory and input devices without use of microprocessor
c) transfer of data exclusively within microprocessor register
d) a fast transfer of data between microprocessor and input device
= Answer (b) direct transfer of data between memory and input devices without use of microprocessor

17) An assembler for a microprocessor is used
a) assembly of processors in a production line
b) creation of new programs using different modules
c) translation of a program from assembly language to machine language
d) translation of higher level language into english text
= Answer (c) translation of a program from assembly language to machine language

18) In an 8085 μP system,the RST instruction will cause an interrupt
a) only if an interrupt service routine is not being executed
b) only if a bit in the interrupt mask is made 0
c) only if interrupt have been enabled by an EI instruction
d) None of the above
= Answer (c) only if interrupt have been enabled by an EI instruction

19) The instruction that does not clear the Accumulator of 8085,is
a) XRA A b) ANI 00H c) MVI A,00H d) None of these
= Answer (d) None of these

20) An input processor controls line flow of information between
a) cache memory and input device
b) main memory and input device
c) two input devices
d) cache and memories
= Answer (b) main memory and input device

21) The number of hardware interrupt (which require an external signal to interrupt) present in an 8085 microprocessor are
a) 1 b) 4 c) 5 d) 13
= Answer (c) 5

22) In the 8085 microprocessor,the RST 6 instructions transfer the program execution to the location
a) 30 b) 24H c) 48H d) 60H
= Answer (a) 30

24) In a microprocessor,the service routine for a certain interrupt starts a fixed location of memory which cannot be externally set but the interrupt can be delayed or rejected.Such an interrupt is
a) non-maskable and non-vectored b) maskable and non-vectored
c) non-maskable and vectored d) maskable and vectored
= Answer (d) maskable and vectored

25) In a 8085 microprocessor system memory mapped I/O,
a) I/O devices have 8 bit addresses
b) arithmetic and logic operations can be directly performed with the I/O data

c) there can be maximum of 256 input devices and 256 output devices
d) I/O devices are accessed using IN and OUT instructions
= Answer (b) arithmetic and logic operations can be directly performed with the I/O data